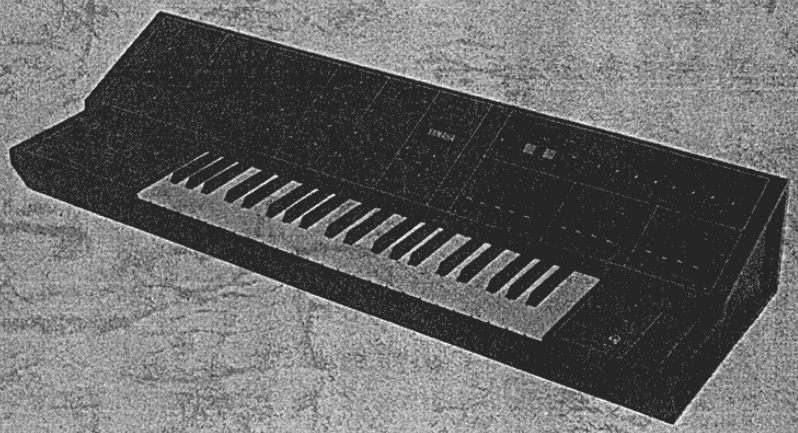
CCS30

YAMAHA

COMBO SYNTHESIZER

CS-30



SERVICE MANUAL

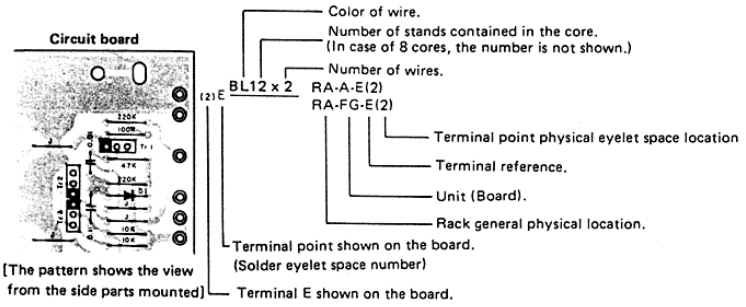
007231

'77 12 1.5K H.K. ® Printed in Japan.

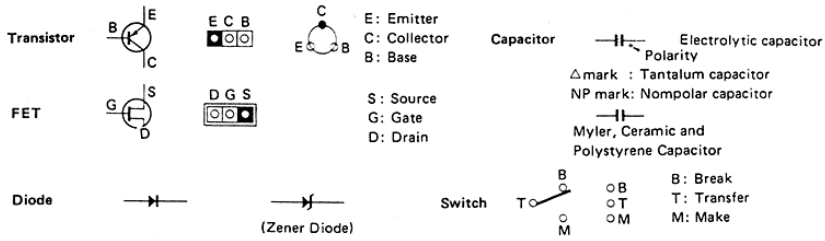
CORDING GUIDE (活用の手引)

1 CIRCUIT BOARD AND WIRING

Two (2) black wires are connected to "E" on circuit board. One goes to each "E" terminal of A and FG circuit boards. In this case, the coding system is as follows:



2 SYMBOL DESCRIPTION



3 ABBREVIATIONS OF WIRE COLOR IN ELECTONE

BLACK	BL	BROWN	BR	RED	RE
ORANGE	OR	YELLOW	YE	GREEN	GR
BLUE	BE	VIOLET	VI	GRAY	GY
WHITE	WH	GRASS GREEN	GG	SKY BLUE	SB
PINK	PK	TRANSPAENT	TR		

4 WIRE COLOR -- Musical Note Indication

C	C#	D	D#	E	F	F#	G	G#	A	A#	B
BR	RE	OR	YE	GR	BE	VI	GY	WH	GG	SB	PK

5 LOGIC SYMBOL

	MIL	YAMAHA
NOT	A — Y	A — Y
NOR	A, B — Y	A, B — Y
NAND	A, B — Y	A, B — Y

Exlusive OR

Truth Table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0

NOT (Inverter)

Truth Table

A	Y
0	1
1	0

OR

Truth Table

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

NOR

Truth Table

A	B	Y
0	0	1
1	0	0
0	1	0
1	1	0

AND

Truth Table

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

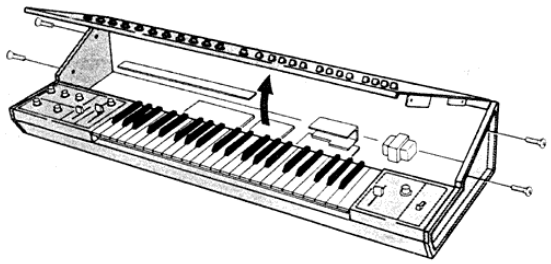
NAND

Truth Table

A	B	Y
0	0	1
1	0	1
0	1	1
0	0	0

DISASSEMBLY PROCEDURE (分解手順)

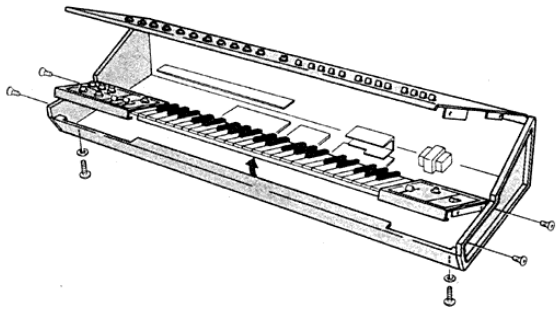
Removal of Panel
パネルの取り外し



Remove all screws illustrated above and take away the panel, lifting it up gently.

図の各ネジを外し、パネルを上へ持ち上げながら取り外して下さい。

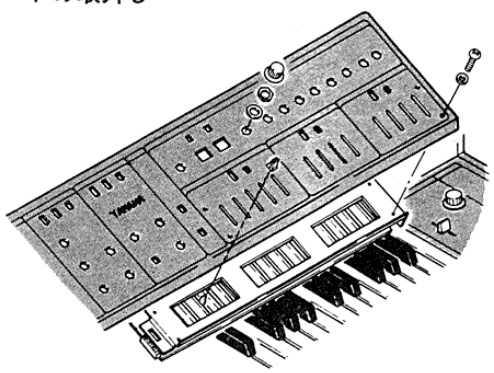
Removal of Keyboard
鍵盤の取り外し



After removing the panel, pulling out the screws as shown above permits rotating the keyboard.

パネルを取り外し後、図の各ネジを外しますと鍵盤を回転させる事ができます。

Removal of Circuit Boards
シートの取外し



Take the circuit boards away gently from the panel, removing each volume knob and hexagonal nut without any damage or scratch on the panel.

パネルを傷付けない様に各ボリウムのつまみと六角ナットを外して、シートをパネルから静かに外して下さい。

SPECIFICATIONS (総合仕様)

Keyboard . . . . . 44 keys, 3½ octaves

CONTROLS

PITCH . . . . . TUNE: +65 cents to –65 cents
DE TUNE; VCO 1: +700 cents to –500 cents
EG: SELECTOR, DEPTH

VCO . . . . . KEY VOLT: SEQ/KBD
FEET;
VCO 1: 2' 4' 8' 16' 32' 64'
VCO 2: 4' 8' 16' 32' 64' 128'
PW: 50~90%
PWM: 10 ~ 90% (LFO sine)
MOD VCO 2 (VCO 1)
MODULATION: FUNCTION, DEPTH

VCF . . . . . VCF1 INPUT: ⋀/⊓ VCO1/⋀ VCO LEVEL
VCO2/NOISE/ EXT LEVEL
VCF2 INPUT: VCF1H/⋀/⊓ VCO2
KBD FOLLOW
MODULATION: FUNCTION, DEPTH
CUT OFF FRQ
RESONANCE
EG: SELECTOR, DEPTH

VCA . . . . . FILTER: HP/BP/LP
VCA 1; Input selectors: VCF 1, VCF 2 and ∿VCO 1
RMO(VCA2): NORMAL/RMO VCO1/LFO
HOLD: HOLD/EG
EG selector: A, C and E
MODULATION: FUNCTION, DEPTH

TRIGGER . . . . . LFO/NORMAL, SINGLE/MULTI

SEQUENCER . . . . . CLOCK SPEED: 0.1~30Hz
STEP: 1 to 8
NORMAL/KBD
CLOCK/MANUAL
MANUAL/START or STOP
HOLD
PITCH: 1 to 8

EG . . . . . TRIGGER: KBD/SEQ/EXT
EG TIME: NORMAL/TIMEx5
EG 1; IL . . . 0 ~ –5
AL . . . 0 ~ +5
AT . . . 1msec.~ 1sec.
DT . . . 10msec.~10sec.
RT . . . 10msec.~10sec.
EG2, 3; AT . . . 1msec.~1sec.
DT . . . 10msec.~10sec.
SL . . . 0 ~ 10
RT . . . 10msec.~10sec.

LFO . . . . . EG: FUNCTION, DEPTH
SPEED: 0.1 ~ 100Hz

EXTERNAL . . . . . Sensitivity: 0/–20 (dBm)
TRIGGER LEVEL: Trigger ON at 60m$V_{p\text{-}p}$ (Min.)
SIGNAL LEVEL

PORTAMENTO . . . . 4sec. at LONG

PITCH BEND . . . . . ±1 octave at LIMITTER max.

OUTPUT . . . . . BALANCE, VOLUME

TERMINALS

OUTPUT . . . . . 1, 1+2, 2;
HIGH: 0dBm/600Ω
LOW: –20dBm/600Ω

FOOT CONTROLLER . . . . for volume control

SEQUENCER OUT . . CONTROL VOLT, TRIGGER

KEY VOLT . . . . . IN/OUT

TRIGGER . . . . . IN/OUT

EXTERNAL . . . . . IN

PHONES . . . . . for headphones

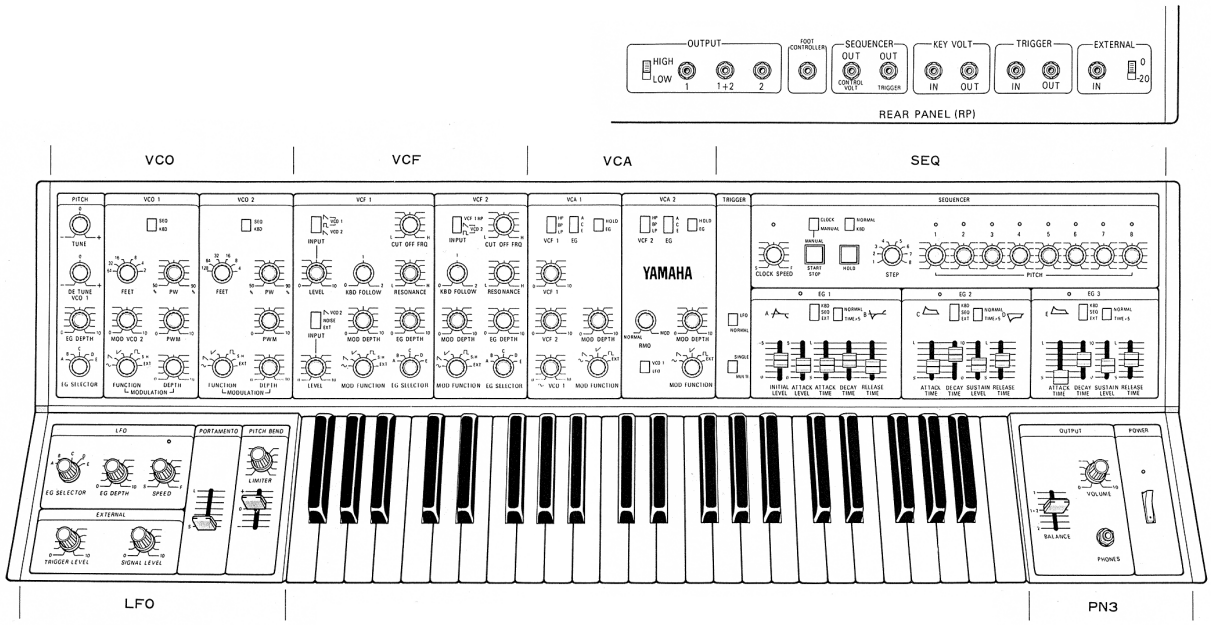
POWER SOURCE: . . . . . AC 50/60 Hz

POWER CONSUMPTION: 40W

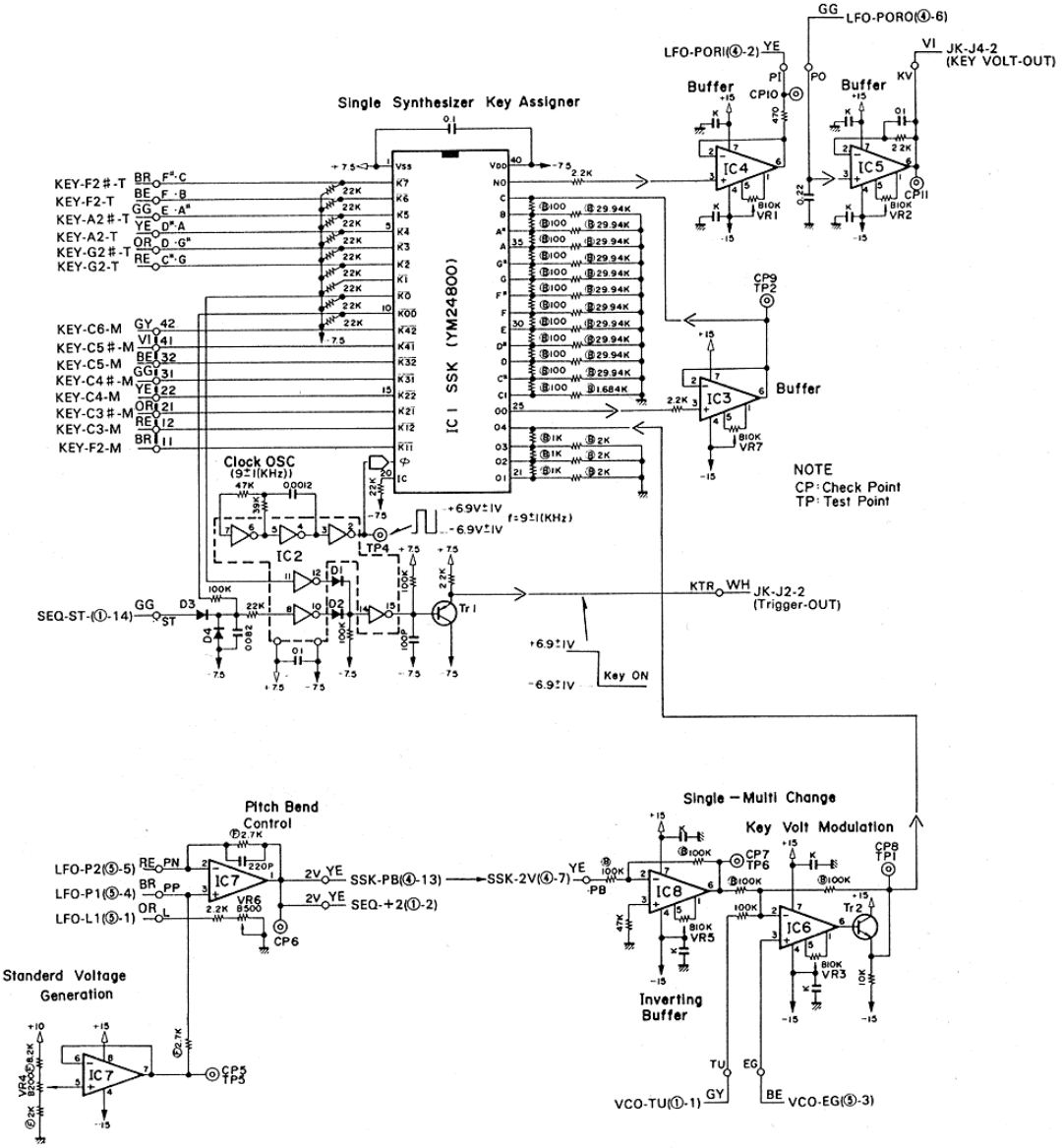
DIMENSIONS . . . . . 978(W) x 330(D) x 173(H) mm
38½(W)x13(D)x6-13/16(H) in.

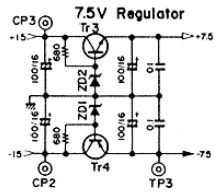
WEIGHT . . . . . 15kg, 33.0 lbs

PANEL LAYOUT（パネルレイアウト）



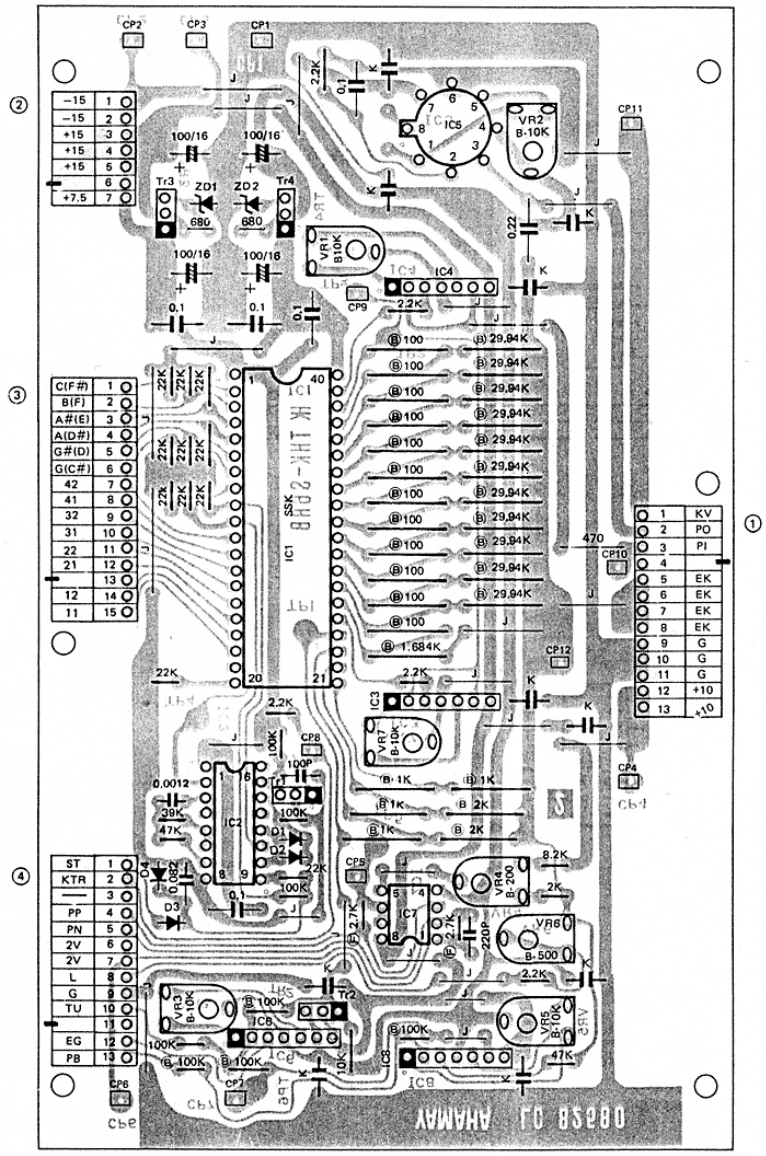
SSK Circuit Diagram





IC1	: YM24800
IC2	: TC4049P
IC3,4,6,8	: TA7504S
IC5	: TA7505M
IC7	: NJM4558DN
Tr1,4	: 2SA561
Tr2,3	: 2SC458
Diodes D1~D4	: 1S1555
ZD1,2	: 02Z7.5A
Ⓕ marks	: 1%
Ⓑ marks	: 0.1%

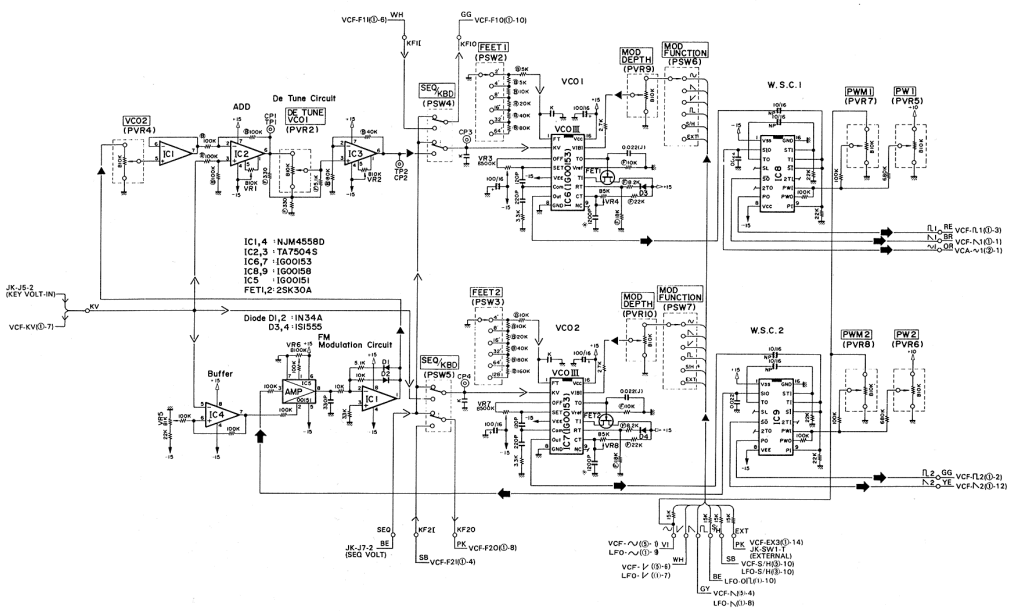
SSK Circuit Board & Wiring



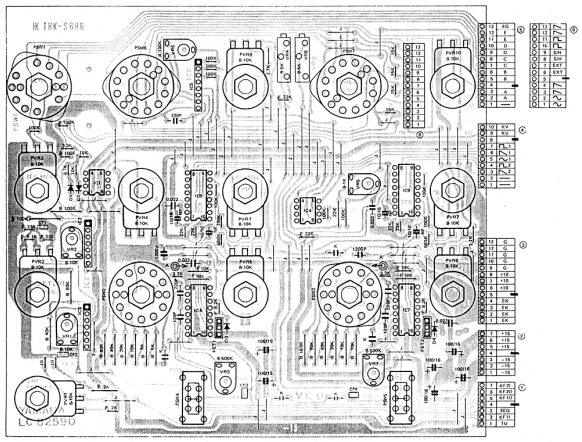
(Note)

1. IC
   - ICI : YM24800
   - IC2 : TC4049
   - IC3,4,6,8 : TA7504
   - IC5 : TC7505
   - IC7 : NJM4558
2. Transistor (トランジスタ)
   - Tr1,4 : 2SA561
   - Tr2,3 : 2SC458
3. Resistor (抵抗)
   - Ⓕ marks : ±1%
   - Ⓑ marks : ±0.1%
4. Diode(ダイオード)
   - ZD1,2 : 02Z7.5A
   - D1～4 : 1S1555
5. Semi variable resistor(半固定抵抗)
   V8K4-1 Type

VCO Circuit Diagram



VCO Circuit Board & Wiring



View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

(Note)

1. IC
   - IC1, 4 : NJM4558DN
   - IC2, 3 : TA7504S
   - IC6, 7 : IG00153
   - IC8, 9 : IG00158
   - IC5 : IG00151
2. FET
   - FET1, 2 : 2SK30A
3. Diode
   - D1, 2 : 1N34A
   - D3, 4 : 1S1555
4. Resistor
   - Ⓑ marks : 0.1%
   - Ⓕ marks : 1%

VCO III (IG00153)

This IC is used for voltage controlled oscillator.
Many defferent frequencies are produced by the voltage supplied.

1. FT ..... Resistor for determination of the feet. The electric current is provided to the pin from transposition changing circuit so that the octave can be determined.
2. KV ..... Input of the key voltage
   The input of the voltage is provided to the pin in corporation with the keys held down.
   High voltage ..... High frequency
   Low voltage ..... Low frequency

(ex.)

Input Voltage	Output Frequency
0.250V	130.8Hz (C2)
0.500V	261.6Hz (C3)
1.000V	523.2Hz (C4)
2.000V	1046.0Hz (C5)
4.000V	2093.0Hz (C6)

Transposition "normal"

3. OFF-SET .... Zero adjustment of input buffer circuit
4. OFF-SET .... Zero adjustment of input buffer circuit
5. Vee ..... −15V input power source.
6. Com .... Phase compensation for input buffer amplifier.
   Normally, the output (KV + 1V) is supplied to the pin.
7. OUT .... Output

As to the frequency, refer to the Pin No.2 (KV).

8. GND .... Earth
9. Vref ..... Input of the standard voltage.
10. CT ..... Circuit for time constant.

The following wave shape is produced.

11. RT ..... Circuit for time constant.

Determines the discharging voltage level.

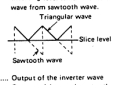
12. T1 ..... Input for the comparator.
    Input of the wave shape (⋀⋀) is provided. from the pin no. 14 (TO).
13. Iref ..... Input of the standard electronic current
14. TO ..... Output from time constant circuit.
    ⋀⋀ The following wave shape is produced.
15. VIB ..... Input for vibrato control wave.
16. Vcc ..... +15V input power source.

WSC IC (IG00158)

1. Vcc ..... +15V input power source
2. SIO ..... Output of the sine wave

3. TO ..... Output of triangular wave.

4. SL ..... Input of slice level.
   Input of the DC voltage is provided to the pin for determination of the inverting level which makes triangular wave from sawtooth wave.



5. $\overline{SO}$ ..... Output of the inverter wave
   Output of inverted sawtooth wave is produced.

6. 2TO ..... Output of double triangle wave
   Double triangle wave is produced from triangle wave.
7. PO ..... Output of pulse wave.

8. Vee ..... −15V input power source.
9. PI ..... Input of pulse wave
   Input of sawtooth wave is provided.

10. PWO ..... Output of OP amplifier.
11. PWI ..... Input of OP amplifier.

Input of the voltage is provided for determination of the sensitivity of PWM lever so that the pulse width is changed.

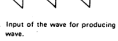
12. 2TI ..... Input of triangular wave for producing double triangular wave shape.

Input of triangular wave (TO) is provided for making double triangular wave shape.

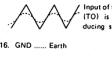
13. $\overline{ST}$ ..... Input of the pulse for producing inverted sawtooth wave.

Input of the sawtooth wave is provided from VCO III for producing inverted sawtooth wave shape.

14. TI ..... Input of the wave is provided for producing triangular wave shape.



15. STI ..... Input of the wave for producing sine wave.



Input of the triangular wave (TO) is provided for producing sine wave.

16. GND ..... Earth

VCF IC (IG00156)

1. AI ..... Signal Input
   Input signals from VCO are provided to this pin.
2. KV ..... Key voltage input
   In order to change the tone color according to the tone range of keyboard, the degignated voltage of the key will supplied to the pin. (0.25-4.0V)
3. fc ..... Adjustment of the cut off frequency.
   Set the control currency of the cut off frequency.
4. Vf ..... Input of the cut off voltage.
   Input voltage of cut off frequency is supplied to this pin so that the tone color can be changed. The center point of the cut off frequency can be also set.
   When the VK is 0.25V and Vf is 5V, the cut off frequency is set to just 1KHz.
5. Vcc ..... +15V input power source
6. Q0 ..... Q adjustment.
   The Q control current sets the Q equal to 10, when VQ is 0 volt.
7. VQ ..... Input of the voltage for Q control. Q is variable according to the control voltage supplied.
   When the control voltage is 0V (Max.), Q=10
   When the control voltage is 10V (Min.), Q=0.5
8. GND .... Earth
9. FB ..... Q feed back
   This is the feed back output pin for the Q control by which the Q is determined.
10. LP ..... Low-pass output

The output of lower frequencies are produced.

11. C2 ..... C pin for determination of the cut off frequency.
12. Vee ..... −15V power source.
13. BP ..... Band-pass output.

The output of intermediate frequences are produced.

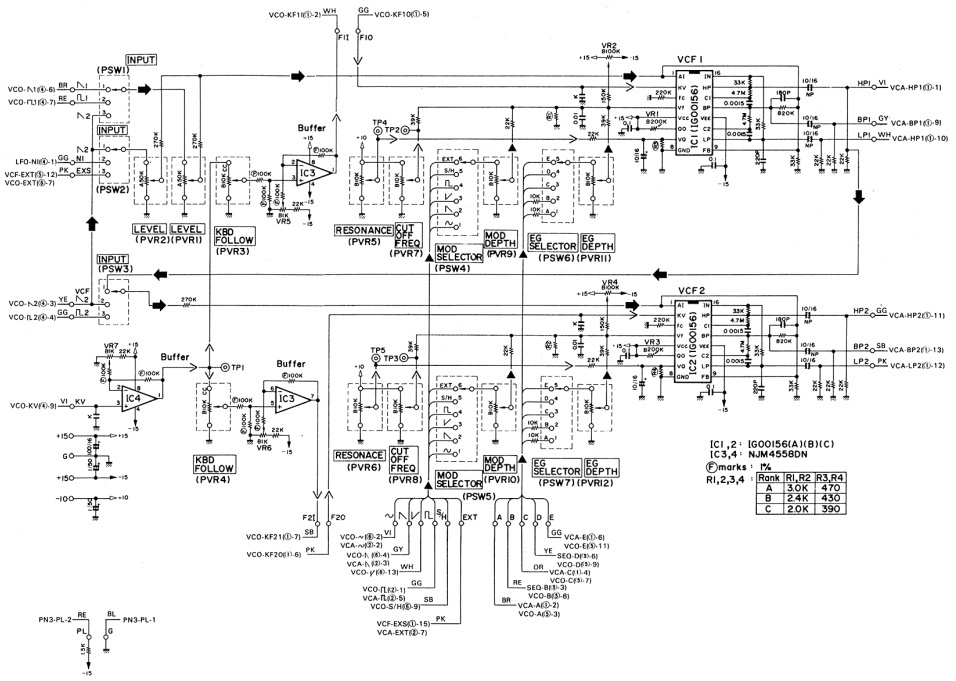
14. C1 ..... C pin for determination of the cut off frequency.
15. HP ..... Hi-pass output

The output of higher frequencies are produced.

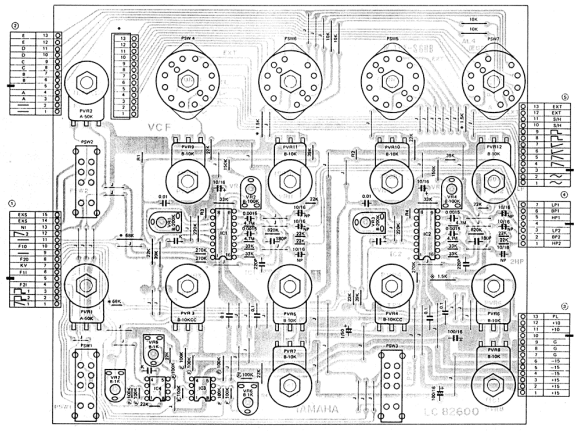
16. IN ..... Input of feed back
    The input signal for determination of cut off frequency.

←- - -Explanation for IC (ＩＣ説明)

VCF Circuit Diagram



VCF Circuit Board & Wiring



* mark : CS-30L only
# mark : CS-30 only

View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

(Note)
1. IC
   IC1,2 : IG00156
   IC3,4 : NJM4558
2. Resistor
   Ⓕ marks : ±1%
   R1R2R3R4 : Rank of IC1,2

IC Rank	R1R2	R3R4
A	3K	470
B	2.4K	430
C	2K	390

KEP-NA 80290-78⚠

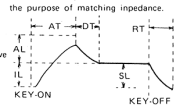
VCF-EG (IG00152)

This IC generates envelope wave shape which is supplied to VCF and control the tone color.

1. NC ..... Not connected
2. BI ..... Input of buffer amplifier.
3. OUT .... Output of buffer amprifier.

   The buffer amplifier is built in for the purpose of matching inpedance.

Output wave shape

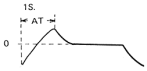


4. GND .... Earth
5. Vcc ..... +15V input power source.
6. G1 ..... Gate 1
7. G2 ..... Gate 2

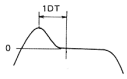
AT starting data

Key ON-OFF data

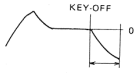
8. Vee ..... −15V input power source.
9. AT ..... Input of buffer voltage for determination of the attack time.
   Input of the voltage between zero V and 10V is provided and the attack time is controlled from 1 mS until 1S.



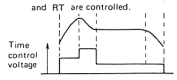
10. DT ..... Input of buffer voltage for determination of the decay time.
    Input of the voltage between zero V and 10V is provided and the first decay time is controlled from 10mS until 10 S.



11. RT ..... Input of buffer voltage for determination of the release time.
    Input of the voltage between zero V to 10V is provided and the time from KEY-ON until release is controlled from 10m second until 10 second.

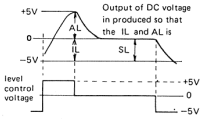


12. TC ..... Output of the time control.
    Output of DC voltage is produced so that the each time of attack, DT and RT are controlled.



The higher the voltage, the shorter the time and the lower the voltage the longer the time.

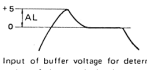
13. LC ..... Output of level control.



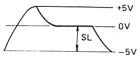
Output of DC voltage in produced so that the IL and AL is

The higher the voltage, the higher the level and the lower the voltage the lower the level.

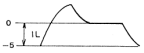
14. AL..... Input of butter voltage for determination of attack level.
    Input of the voltage between (0V~10V is provided and the attack level is controlled from 0V until +5V.



15. SL ..... Input of buffer voltage for determination of the sustain level.
    Normally fixed to zero(0) volt.



16. IL ..... Input of buffer voltage for determination of the initial level.
    Input of the voltage between zero 0V and ten 10V is provided and the initial level is controlled from zero to minus 5 volt.



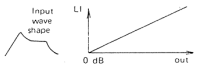
→ – –Explanation for IC
(ＩＣ説明)

VCA Circuit Diagram

VCA IC (IG00151)

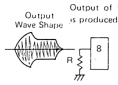
1. EI ..... Input voltage for level control.
   Input of the control voltage is provided for changing the level expotenentially.

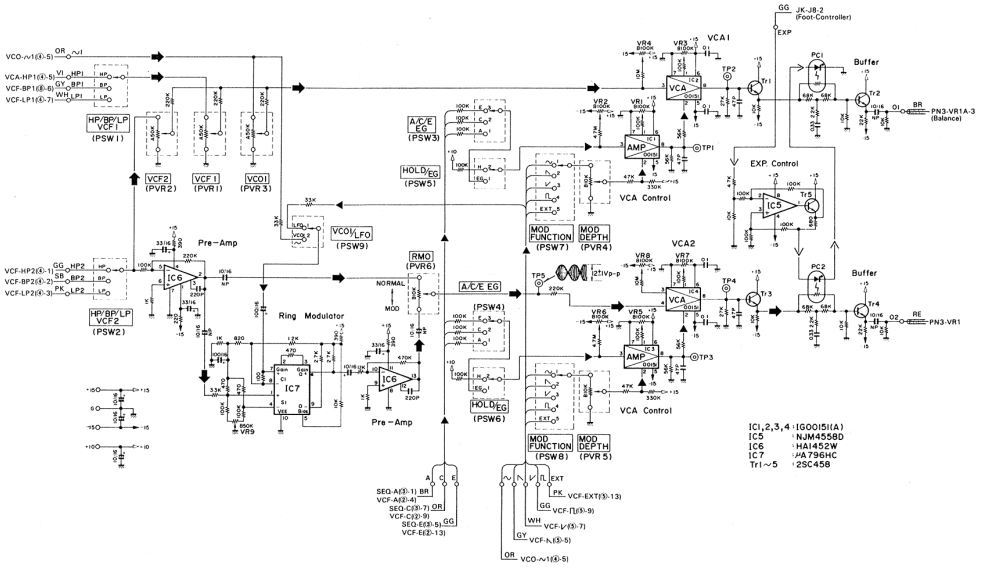
2. LI ..... Input of level control voltage.
   Input of the control voltage is provided for linear change of the level.



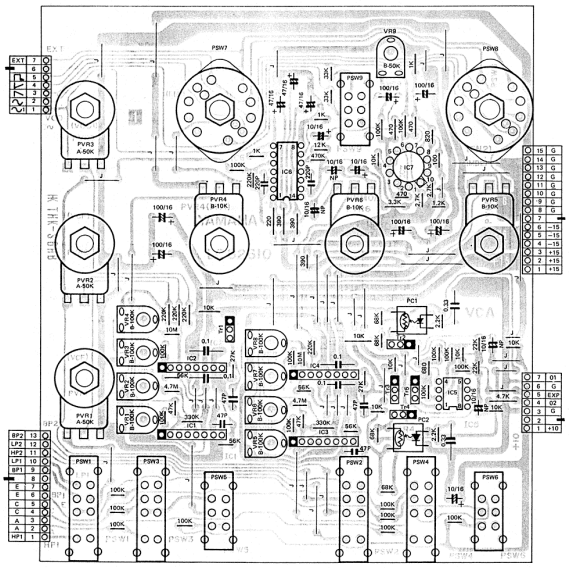
3. +IN ..... Input
   Input of the level modulated signal is provided.

4. –IN ..... Negative feed back.
   Normally unused.
5. Vee ..... –15V input power source.
6. Vcc ..... +15V input power source.
7. GND ..... Earth
8. OUT ..... Output
   Output of the following wave shape is produced.





VCA Circuit Board & Wiring



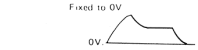
View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

(Note)
1. IC
   IC1 ~ 4 : IG00151
   IC5 : NJM4558
   IC6 : HA1452
   IC7 : μA796HC
2. Transistor (トランジスタ)
   Tr1 ~ 5 : 2SC458
3. Photo coupler
   PC1 - 2 : P558-G50-201B
4. Semi Variable Resistor (半固定抵抗)
   UR1 ~ 9 : V8K-4-1 Type

VCA-EG IC (IG00159)

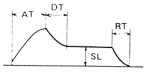
This IC generates envelope wave shape which is supplied to VCA and control the tone volume.

1. IL ..... Input of initial level.

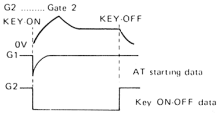


2. BI ..... Input of buffer amplifier.
3. OUT ... The buffer amplifier is built in for the purpose of matching impedance.

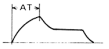
Output wave shape.



4. GND ..... Earth
5. Vcc ..... +15V input power source.
6. G1 ..... Gate 1
7. G2 ..... Gate 2

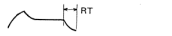


8. Vee ..... +15V input power source.
9. AT ..... Input of buffer voltage for determination of attack time.
   Input of the voltage between zero V and 10V is provided and the attack time is controlled from 1 mS until 1S.

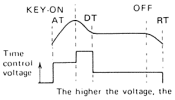


10. 1DT ..... Input of buffer voltage for determination of decay time.
    Input of the voltage between zero V and 10V is provided and the decay time is controlled from 10 m second until 10 second.

11. 2DT ..... Input of buffer voltage for determination of release time.
    Input of the voltage between zero V and 10V is provided and the time key-off untill release is controlled from 10 mS until 10 S.

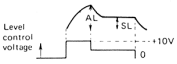


12. TC ..... Output of time control.
    Output of the DC voltage is produced so that the each time of Attack, 1st Decay and 2nd Decay are controlled.



The higher the voltage, the shorter the time and the lower the voltage, the longer the time.

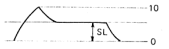
13. LC ..... Output of level control



Output of the DC voltage for AL and SL control is provided.

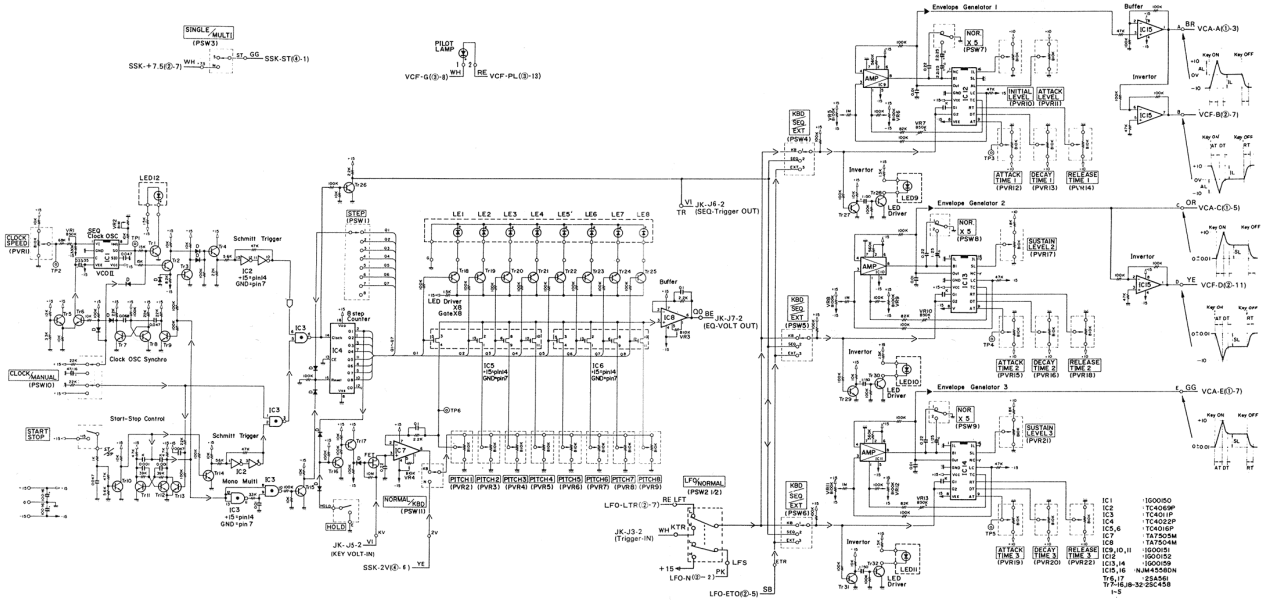
The higher the voltage , the higher the level and the lower the voltage, the lower the level.

14. NC..... Not connected.
15. SL ..... Input of buffer voltage for determination of the sustain level.
    Input of the voltage between zero V and 10V is provided so that the sustain level can be controlled.

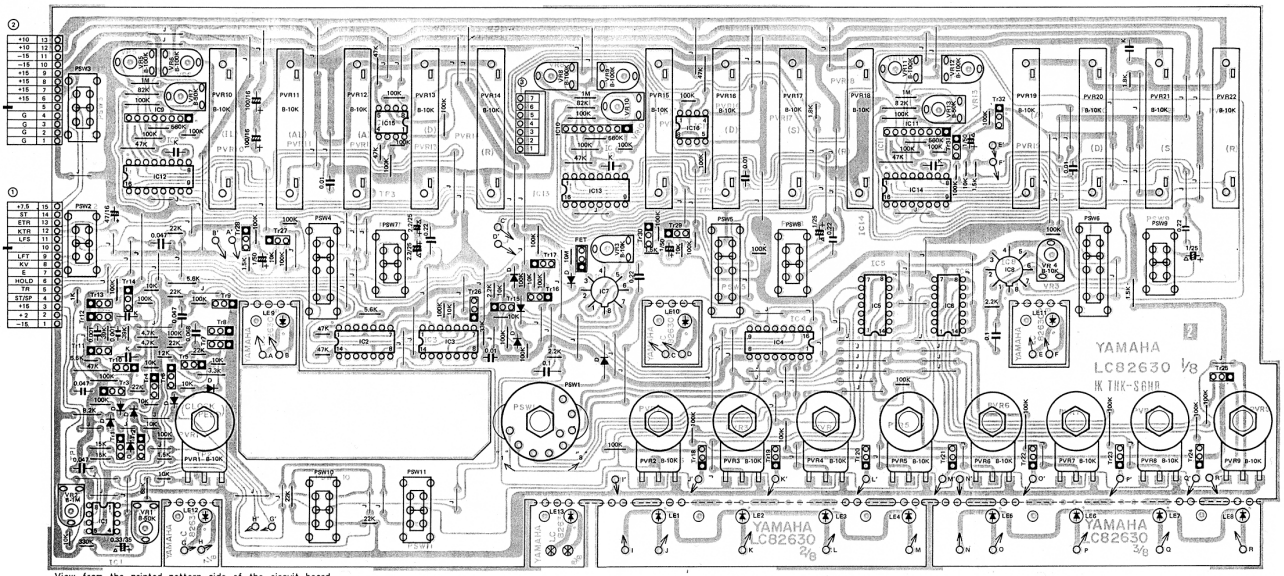


16. NC ..... Not connected.

SEQ Circuit Diagram



SEQ Circuit Board & Wiring

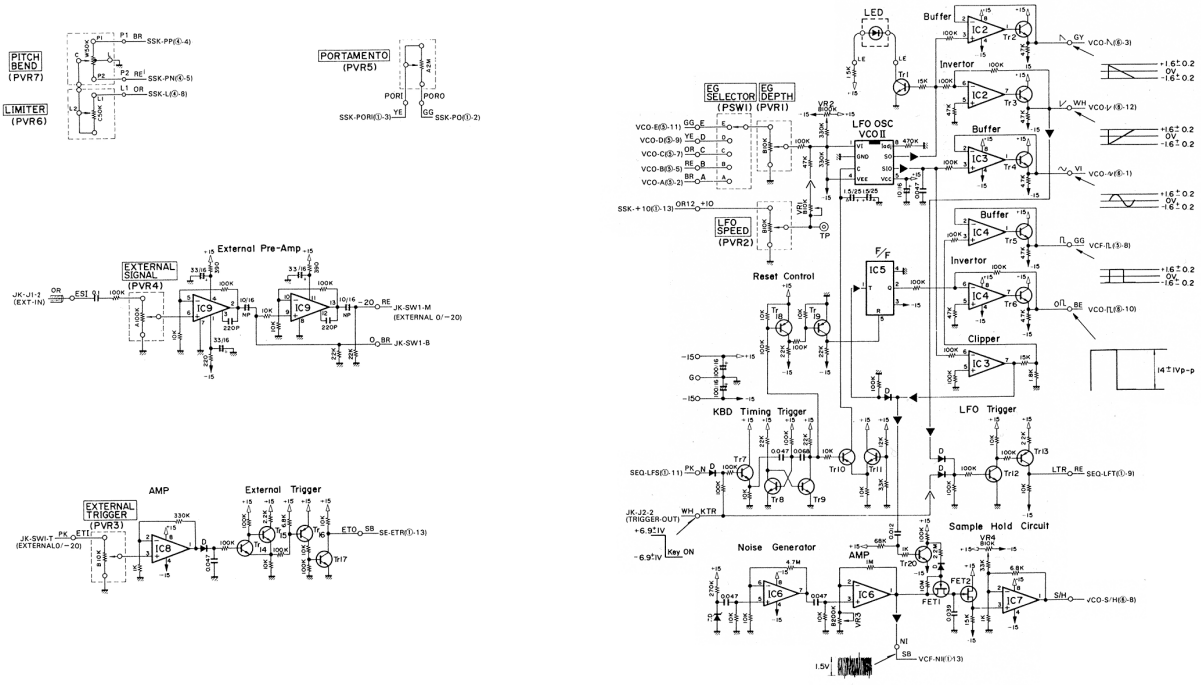


View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

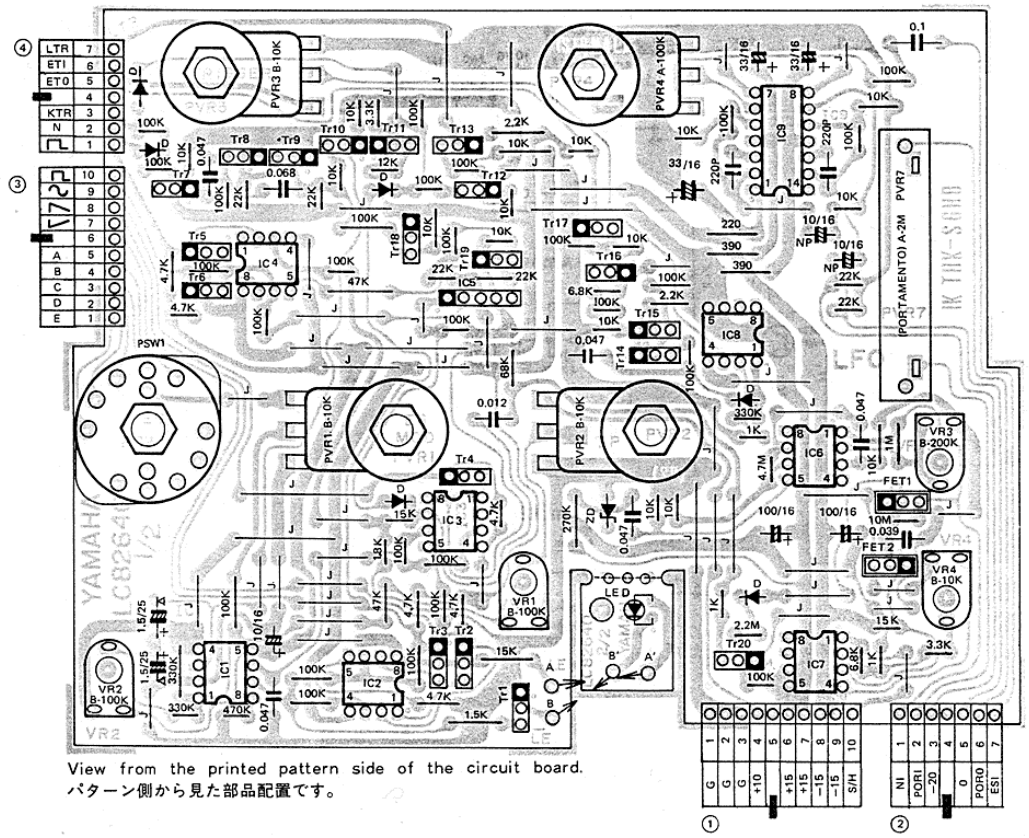
(Note)
1. IC
IC1	: IG00150
IC2	: TC4069P
IC3	: TC4011P
IC4	: TC4022P
IC5,6	: TC4016P
IC8	: TA7504M
IC9～11	: IG00151
IC12	: IG00152
IC13,14	: IG00159
IC15,16	: NJM4558
IC7	: TA7505M

2. Transistor (トランジスタ)
   Tr6,17 : 2SA561
   other : 2SC458
3. FET : 2SK30A
4. Diode (ダイオード)
   D : 1S1555
5. LED (発光ダイオード)
   SLP1328

LFO Circuit Diagram



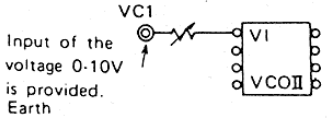
LFO Circuit Board & Wiring



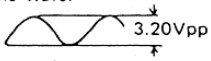
View from the printed pattern side of the circuit board.
パターン側から見た部品配置です。

VCO II (IG00150)

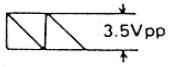
1. VI ..... Input of the control voltage.
   The frequency is variable in accordance with the voltage supplied.



2. GND ..... Earth
3. C ..... Capacitor for determination of the frequency.
4. Vee ..... −15V input power source.
5. Vcc ..... +15V input power source.
6. SIO ..... Output of sine wave.



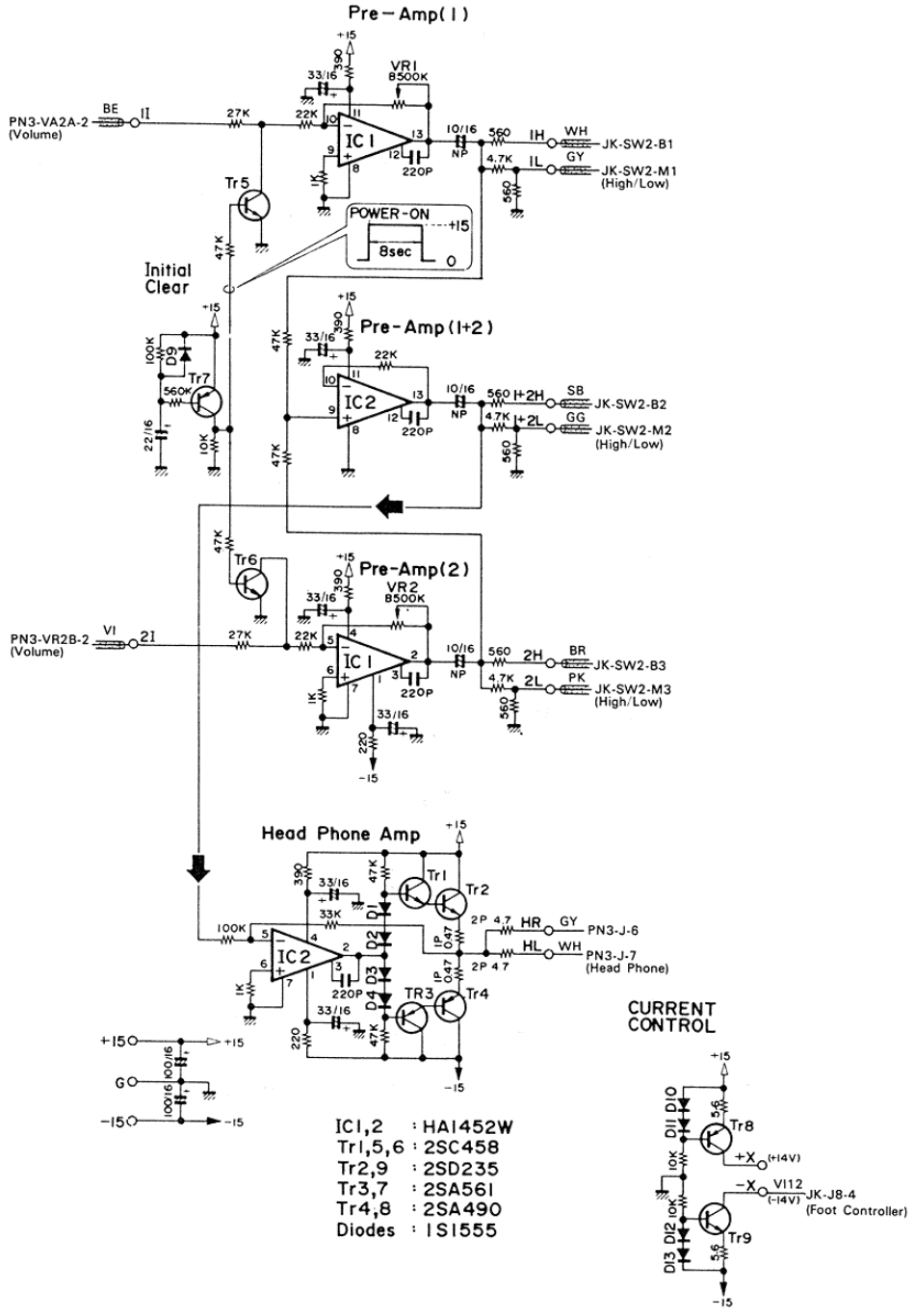
7. SO ..... Output of sawtooth wave



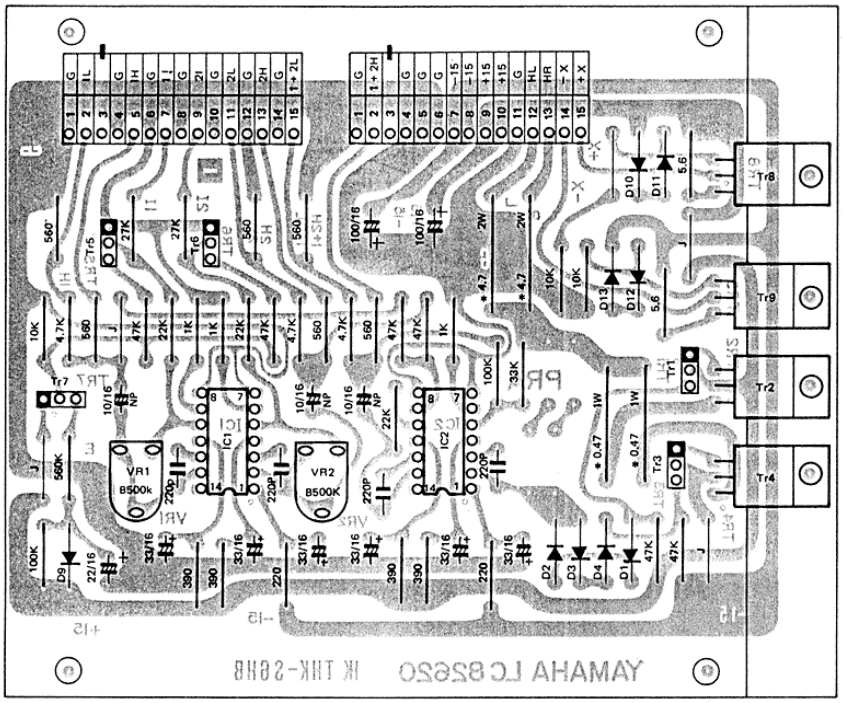
8. Iadj ..... Setting for standard electric current.

(Note)
1. IC
   IC1 : IG00150
   IC5 : BA634
   IC9 : HA1452
   IC2～4, 6～8 : NJM4558
2. Transistor (トランジスタ)
   Tr1～9, 11,12,14,15,17,20 : 2SC458
   Tr10,13,16,18,19 : 2SA561
3. Diode (ダイオード)
   D : 1S1555
   ZD : 1S1715
4. FET
   FET1,2 : 2SK30A

PRA Circuit Diagram



PRA Circuit Board & Wiring

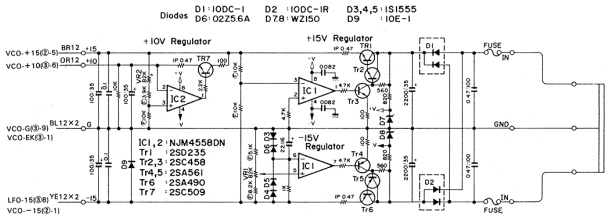


(Note)

1. IC
   IC1,2 : HA1452
2. Transistor (トランジスタ)
   Tr1,5,6 : 2SC458
   Tr2,9 : 2SD235
   Tr3,7 : 2SA561
   Tr4,8 : 2SA490
3. Diode (ダイオード)
   D1～13 : 1S1555
4. Semi Variable Resistor (半固定抵抗)
   VR1,2 : V8K-4-1
5. Metal oxide film resistor (酸金抵抗)
   * marks:

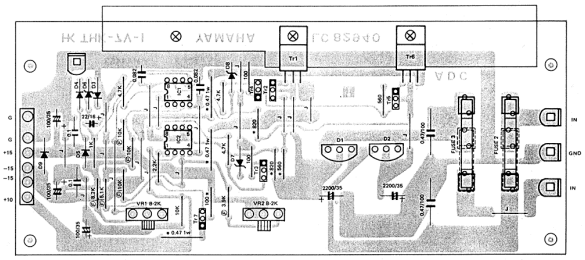
CS-30(S/# 1001~)

ADC Circuit Diagram



KEC-10114-77⚠

ADC Circuit Board & Wiring

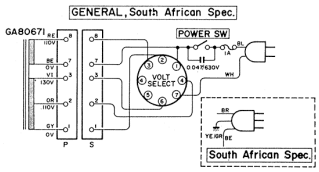


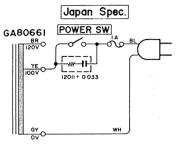
(Note)

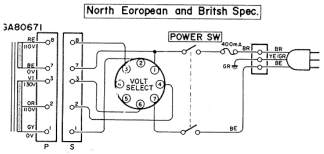
1. FUSE 2・3
   Japan . . . . . 1.5 AT
   N.European, BS . . . 1.6 AT (mini)
   other . . . . . 1.5 AT (UL)
2. Transistor (トランジスタ)
   Tr1 : 2SD235
   Tr2,3 : 2SC458
   Tr4,5 : 2SA561
   Tr6 : 2SA490
   Tr7 : 2SC509
3. Diode
   D1 : 10DC-1
   D2 : 10DC-1R
   D3,4,5 : 1S1555
   D6 : 02Z5.6A
   D7,8 : WZ150
   D9 : 10E-1
4. IC
   IC1,2 : NJM4558
5. Resistor (抵抗)
   mark : 1%
   0.47Ω 1W : Metal oxide film (酸金抵抗)
   * mark :

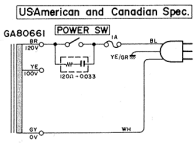
6. Semi variable resistor (半固定抵抗)
   RV1,2 : V18K Type B-2KΩ

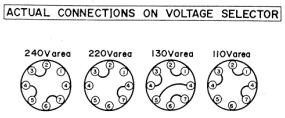
KEP-NA 80296-78⚠

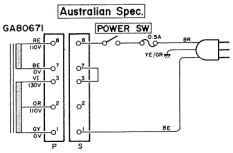




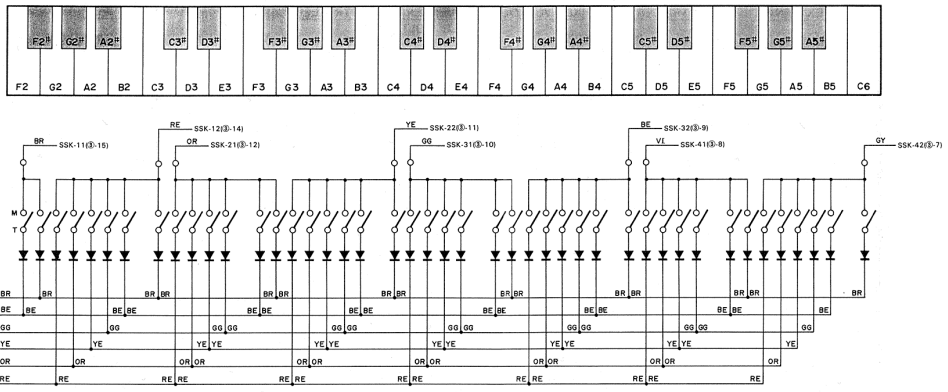






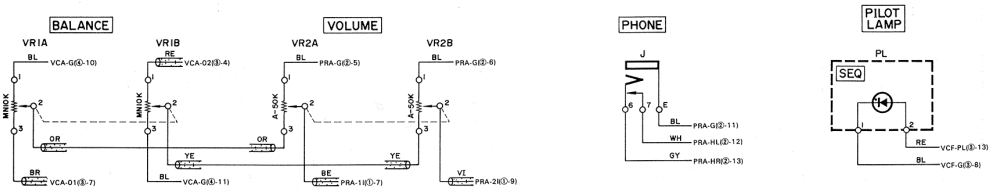


KEY SWITCH Circuit Diagram



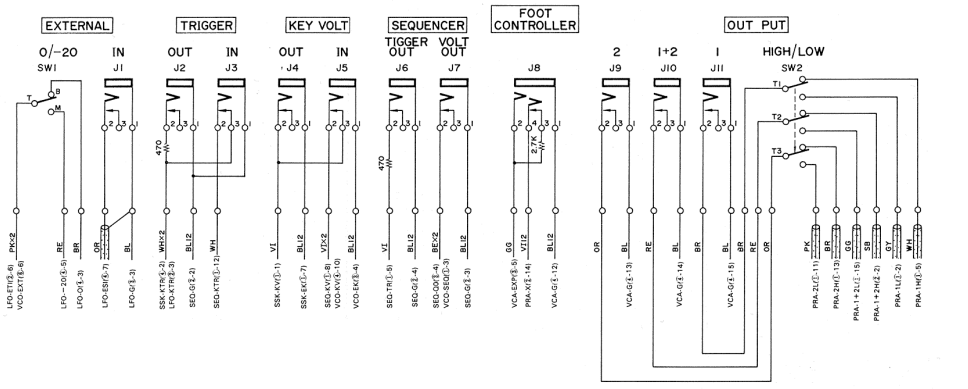
KEC-90113-78⚠

PN3 Circuit Diagram



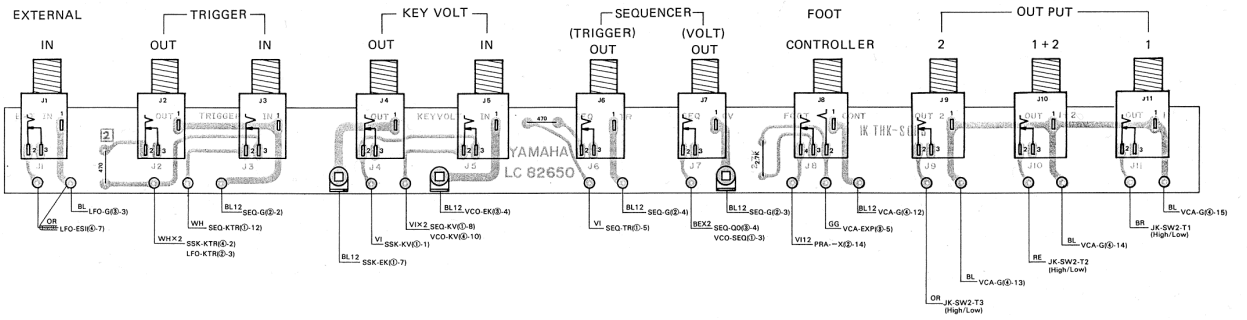
KEC-90113-78⚠

REAR PANEL Circuit Diagram (JK)



KEC-90113-78 ⚠

REAR PANEL Circuit Board & Wiring



KEP-NA80295-78 ⚠

Standerd for circuit inspecpion and adjustment

ADC Circuit Board

1. −15V Adjustment (+15V Adjustment)
   Adjust VR1 until a voltage of −15.00V is present across −15V and E terminals. Then, make sure that a voltage of +15 ± 0.15V is present across +15V and E terminals.

2. +10V Adjustment
   Adjust VR2 until a voltage of +10.00V is present across +10V and E terminals.

3. Load Characteristics
   When no load is applied, the fluctuation should be smaller than ±0.5% and should show neither oscillation nor abnormal voltage.
   Make sure that the regulator's response to load fluctuation is within 50m sec. When connecting Mylar capacitors of 0.47μF across each terminal and the E terminal, make sure that neither oscillation nor abnormal voltage is generated and the response time is within 50m sec.

4. First Stage Voltage and Output Voltage
   When load is fully applied, the output voltage fluctuation should be smaller than ±0.1% for the first stage voltage fluctuation of ±15%, and the regulator should respond within 50m sec to a drastic change in the first stage voltage.

5. Ripple Noise
   When load is fully applied, make sure that ripple noise smaller than 10mVp-p is present at each output terminal.

SSK Circuit Board

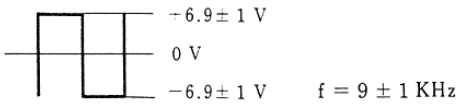
1. Power Supply for Key Assignor

+7V Adjustment . . . . . Make sure that voltage of +6.9 ± 0.6V is present at 1st Pin of IC_1.

−7V Adjustment . . . . . Make sure that voltage of −6.9 ± 0.6V is present at 40th Pin of IC_1.

2. Key Assignor Clock

Make sure that a waveform as in the figure below is obtainable at 2nd Pin of IC_2.



3. Pitch Bend Voltage Generator Circuit

a. Set the PITCH BEND knob to 0 position, then adjust [VR 4] until 2.000V is obtained at CP6 or 2V (④−6.7) terminal.

b. Set the LIMITTER lever to MAX position and PITCH BEND knob to "+" position, then adjust [VR 6] so that 4.000V is obtained at PB (④−13) terminal.

Note: When PITCH BEND knob is in "−" position 1.00V is obtained at PB terminal.

4. Key Voltage Modulator Circuit

a. Set the PITCH BEND knob to 0 position, then adjust [VR 5] so that −2.000V is obtained at CP7.

b. Adjust the TUNE knob until 0.000V is present at TU (④−10) terminal. Set the EG−DEPTH knob in PITCH Section to 0 position, then adjust [VR 3] so that 2.000V is obtained at CP8.

5. Key Voltage Generator Circuit

a. Press F_2 key and adjust [VR 7] so that 250 ± 0.2mV is obtained at CP9.

b. After the item 4−(a) adjustment, adjust [VR 1] so that 166.8 ± 0.1mV is obtained at CP10 or PI (①−3) terminal.

c. After the item 4−(b) adjustment, adjust [VR 2] until 166.8 ± 0.1mV is present at CP11 or KV (①−1) terminal.

6. Portamento Circuit

a. Set the PORTAMENTO lever to S position, press F_2 key, and then turn C_6 key on, make sure that a waveform as in the figure A is obtainable at KV (①−1) terminal.

b. Set the PORTAMENTO lever to L position, then make sure that a waveform as in the figure B is obtainable at the same.

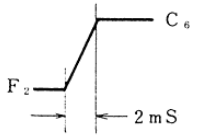


Fig. A

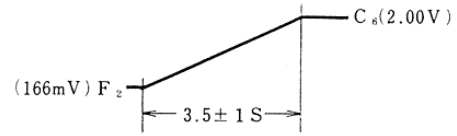
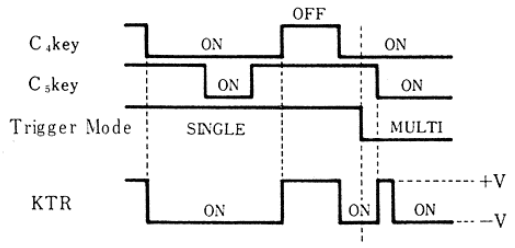


Fig. B

7. Trigger Mode Convertor Circuit

Turn on and off the C_4 and C_5 keys as in the figure below, change the key mode from SINGLE to MULTI, and make sure that the KTR terminal output is as shown in the figure.



During SINGLE Mode, as long as a key remains depressed, operating other keys has no effect on the KTR, which is kept ON.

During MULTI Mode, depressing keys successively permits KTR to turn ON one after another with priority given to higher tones.

c. Leave adjustments as in 2–(b) and use the CUT OFF FREQ (PVR8) to adjust for a TP3 voltage of +7 ± 0.1V. Then turn the B_5 key ON; when the KBD FOLLOW (PVR4) is set for 500mV at the second pin of IC_2 the LP2 level should just peak.
Next, when TP3 voltage is +3 ± 0.1V turn the B_2 key ON. When the KBD FOLLOW (PVR4) is used to set for 500mV at the second pin of IC_2 the LP2 level should peak.

d. Return the setting to the 2–(a, b) condition. When the MOD FUNCTION (PSW5) is set to ∧∨ and MOD DEPTH (PVR10) to 10 check the cutoff frequency by listening to the sound according to the input ∧∨ wave.

e. Set EG1 ~ 3 to any position and EG DEPTH (PVR12) to approximately center position. Peak frequency should vary according to the EG waveform when the EG SELECTOR (PSW12) is switched from A to E.

3. KBD FOLLOW Circuit

a. When the F_2 key is ON (with 166.8mV present at the KV (①–7) terminal), adjust [VR 7] so that 0mV is present at TP1.

b. With the KBD FOLLOW (PVR3) set to 0, adjust [VR 5] so that the F1I (①–6) terminal receives 166.8mV.
Then set the KBD FOLLOW (PVR3) to 1 and turn the C_6 key ON. Check for 2.000V at the F1I (①–6) terminal.

c. As in 3–(a), with the KBD FOLLOW (PVR4) to 0, adjust [VR 6] so that 166.8mV appears at the F2I (①–4) terminal.
Next, set the KBD FOLLOW (PVR4) to 1. Check for 2.000V at the F2I (①–4) terminal when the C_6 key is ON.

VCA Circuit Board

1. Voltage Control Amplifier Circuit No. 1 (VCA1)

a. Set the VCF1 (PVR1), VCF2 (PVR2), ⩘ VCO1 (PVR3) and MOD DEPTH (PVR4) to 0, and set the HOLD/EG switch (PSW5) to HOLD.
Adjust [VR 1], when [VR 2] is at approximately its center position, so that +3 ± 0.1V is present at TP1.
Then set each of the EG1 ~ 3 sliders to either 0 or S and adjust [VR 2] so that −200 ± 10mV is present at TP1 when the HOLD/EG switch (PSW5) is set to EG (i.e., when 0V input is present at the third pin of IC_1).

After the above adjustments, set the HP/BP/LP switch (PSW2) to HP, the MOD FUNCTION (PSW7) to ⩘ and VCF2 (PVR2) to 10.

b. As in 1−(a), set the HOLD/EG switch (PSW5) to HOLD and the VCO2 FEET to 4'. Adjust the CUT OFF FREQ of VCF2 and the RESONANCE so that a 1053Hz, 3Vp-p waveform is input to the HP2 (①−11) terminal when the C_4 key is ON.
At this time adjust [VR 3] so that a 1.3Vp-p waveform is present at TP2.

Next set VCF2 (PVR2) to 0, MOD DEPTH (PVR4) to 10 and LFO SPEED to F. Adjust [VR 4] so that the TP2 output waveform level is minimum when a 100Hz, 3Vp-p wave is added to the ⩘ (②−2) terminal.

2. Voltage Control Amplifier Circuit No. 2 (VCA2)

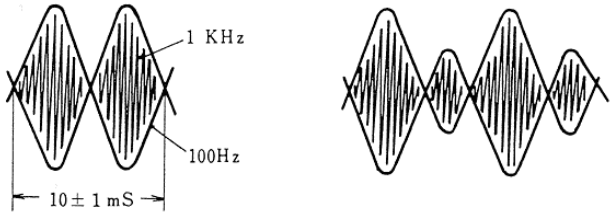
a. Set the MOD DEPTH (PVR5) to 0, MOD FUNCTION (PSW8) to ⩘ and the HOLD/EG switch (PSW6) to HOLD.
When [VR 6] is set to approximately its middle position, adjust [VR 5] so that +3 ± 0.1V is present at TP3.
Then set each of the EG1 ~ 3 sliders to either 0 or S and adjust VR6 so that −200 ± 10mV is present at TP3 when the HOLD/EG switch (PSW6) is set to EG (i.e., when 0V input is present at the third pin of IC_3).

b. As in 2−(a), set the HOLD/EG switch (PSW6) to HOLD, VCO2 FEET to 4' and switch the C_4 key ON. Adjust the VCO2 CUT OFF FREQ and RESONANCE so that a 1053Hz, 3Vp-p waveform is present as input at the HP2 (①−11) terminal. Set the RMO volume (PVR6) to NORMAL. At this time a 6.6 ± 0.3V waveform should appear at TP5.
With everything set in this condition, adjust [VR 7] so that a 1.5 ± 0.05V waveform is present at TP4.
Next set the VCO2 section KBD/SEQ switch to SEQ and turn the SEQ section PITCH 1 all the way to the left (so that 0V appears at the HP2 (①−11) terminal). Also set the LFO SPEED to F. Adjust [VR 8] so that the TP4 output waveform is minimum when a 100Hz, 3V ⩘ waveform is added to the ⩘ (②−2) terminal.

3. RING MODULATOR Circuit

a. Set the VCO1/LFO switch (PSW9) to LFO, the RMO volume (PVR6) to MOD and the KBD/SEQ switch in the VCO2 section to SEQ. Then turn the PITCH 1 of the SEQ section all the way to the left (so that 0V appears at the HP2 (①–11) terminal) and set the LFO section SPEED to F. Adjust [VR 9] so that the TP5 signal is minimum when a 100Hz, 3Vp-p ∧∨ waveform is added to the ∧∨ (②–2) terminal.

b. After the above adjustments are made, return the KBD/SEQ switch of the VCO section to KBD and set the VCO2 FEET to 4'. With the C_4 key ON (i.e., with a 1KHz, 3V waveform added to the HP2 (①–11) terminal), the waveform shown below should appear at TP5.



If the waveform is unbalanced, take its average.

Note: If the waveform is hard to read, adjust the LFO SPEED slightly.

SEQ Circuit Board

1. Clock Pulse Oscillator Circuit

Turn the CLOCK/MANUAL (PSW10) switch to CLOCK and turn the CLOCK SPEED volume (PVR1) to S as far as it will go. Make sure that the frequency is 0.1 ± 0.01Hz at TP1. If not, adjust it by turning [VR 2] . Then, turn the CLOCK SPEED volume fully to F position and adjust [VR 1] until 30 ± 3Hz is obtained. Repeat this adjustment until both S and F levels are both satisfied. LED indicator must glow in accordance with the frequency.

2. Sequencer Circuits

A. Step Circuit

a. After turning the CLOCK/MANUAL (PSW10) switch to CLOCK, STEP (PSW1) selector to 8 and NORMAL/KBD (PSW11) to NORMAL respectively, rotate the CLOCK SPEED volume (PVR1) by about 1/3 of its full extent and depress START/STOP button. The LED indicator should glow to indicate that the steps are shifted from 1 to 8 in sequence.

b. Turn the STEP (PSW1) switch to [n] position and the step must be changed to 1 to [n] from 1 to 8.

B. START/STOP Circuit

After turning the switches as mentioned in paragraph A—(a) above, press START/STOP button ON (+15V input is applied to terminals SP/ST (①—4)). The LED indicator will go off the moment the START/STOP button is depressed and will start from step 1 immediately after the switch is turned ON again.

When CLOCK/MANUAL switch (PSW10) is turned to MANUAL position, the timing step will be halted and it should be shifted step by step turning the START/STOP button ON and OFF alternately.

C. Pitch Circuit

After turning the switches as mentioned in paragraph A—(a), rotate each PITCH volume from 1 to 8 (PVR2 to 9) fully in the counterclockwise direction. Adjust [VR 3] so that the voltage level at terminal Q_0 (③—4) is 0 ± 50μV. Similarly, when all PITCH volumes are turned fully in the clockwise direction, 2 ± 0.002V should be obtained at the terminal. With an arbitrary setting of each PITCH volume of 1 to 8, a voltage between 0 and +2V in accordance with the setting should be obtained.

D. KV Buffer Circuit

a. Insert an open plug into KEY VOLT—IN receptacle (J5) on the rear panel and short KV (①—8) across G terminal. When NORMAL/KBD switch (PSW11) is turned to KBD position, the voltage at TP6 must be 0 ± 50μV. If not, adjust it by means of [VR 4] .

b. Withdraw the open plug, clear the short circuit and set PITCH 1 (PVR2) volume to the center position. When PITCH volumes 2 to "n" (PVR3 to "n") are fully turned in the clockwise direction, +2 ± 0.002V with the PITCH 1 timing and +4 ± 0.3V with the timing of PITCH 2 to [n] should appear in Q_0 (③—4) terminal.

E. Hold Circuit

When HOLD button is continuously depressed with the same setting as the above paragraph (a), the voltage levels of +2 ± 0.05V with the timing of PITCH 1 and +4 ± 0.3V with the timing of PITCH 2 to n should appear respectively.

3. Envelope Generator Circuit

A. EG1

a. Respectively turn KBD/SEQ/EXT selector switch (PSW4) to KBD, NORMAL/TIME x 5 switch (PSW7) to NORMAL, INITIAL LEVEL lever (PVR10) to −5, ATTACK LEVEL lever (PVR11) to +5 and DECAY TIME (PVR13) and RELEASE TIME (PVR14) levers to S positions.
Turn the ATTACK TIME Lever (PVR12) until +8 ± 0.1V is obtained at TP3. Adjust VR 6 so that the rising curve as shown in Fig. 1 with T of 4 ± 0.1mS is obtained from terminal A (③−1) when the key is ON (−7V is applied to the terminal TR (①−5). In addition, adjust VR 5 so that the voltage is levelled off at 0 ± 0.1V 5 seconds or later after the key has been turned ON.

b. Turn the ATTACK TIME lever until +3V ± 0.1V is obtained at TP3 and turn the key ON. Adjust VR 7 to lengthen T when it is longer than 125mS or to shorten T when it is shorter. Raise the TP3 voltage level to +8 ± 0.1V and adjust VR 8 again to 4 ± 0.1mS. Repeat this adjustment until T becomes 125 ± 5mS when +3 ± 0.1V is applied to TP3.

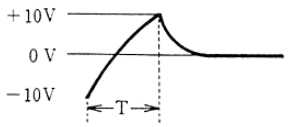


Fig. 1

c. The inverse waveform of terminal A output should be obtained at terminal B (③−3). Confirm that the above T is multiplied by 3.3 to 6.1 when NORMAL/TIME x 5 switch (PSW7) is in TIME x 5 position.
Also make sure that LED indicator (LE9) glows when the key is ON.

B. EG2

a. Respectively turn KBD/SEQ/EXT selector switch (PSW5) KBD, NORMAL/TIME x 5 switch (PSW8) to NORMAL, both DECAY TIME (PVR16) and RELEASE TIME (PVR18) levers to S and SUSTAIN LEVEL lever (PVR17) to 0 positions.
Turn ATTACK TIME lever (PVR15) until +8 ± 0.2V appears at TP4. Adjust VR 9 so that the rising curve as shown in Fig. 2 is obtained from terminal C (③−7) with T of 4 ± 0.1mS when the key is ON (−7V is applied to terminal TR (①−5). Also adjust VR8 so that the voltage is levelled off at 0 ± 0.01V 5 seconds or later after the key is ON.

b. Turn the ATTACK TIME lever until +3 ± 0.1V appears at TP4 and turn the key ON. Adjust VR10 to lengthen T when it exceeds 125mS or to shorten T when it is less than that. Raise the voltage level of TP4 to +8 ± 0.1V and adjust VR 9 again for 4 ± 0.1mS. Repeat this adjustment until T becomes 125 ± 5mS when TP4 is +3 ± 0.1V.

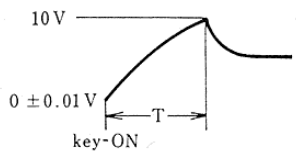


Fig. 2

c. The inverse waveform of terminal C output should be obtained at terminal D (3 –6). Confirm that T above is multiplied by 3.3 to 6.1 when NORMAL/TIME x 5 switch (PSW8) is at TIME x 5 position. Also make sure that LED indicator (LE10) glows when the key is ON.

C. EG3

a. Respectively turn KBD/SEQ/EXT selector switch (PSW6) to KBD, NORMAL/TIME x 5 switch (PSW9) to NORMAL, both DECAY TIME (PVR20) and RELEASE TIME (PSW9) levers to S and SUSTAIN LEVEL lever (PVR21) to 0 positions. Turn ATTACK TIME lever (PVR19) until +8 ± 0.2V appears in TP5. Adjust VR12 so that the above rising curve is obtained from terminal E (③–5) with 4 ± 0.1mS of T when the key is ON (–7V is applied to terminal TR (①–5)). Also adjust VR11 so that the voltage is levelled off at 0 ± 0.01V 5 seconds or later after the key is turned ON.

b. Turn ATTACK TIME lever until +3 ± 0.1V appears in TP5. Adjust VR13 to lengthen T when it exceeds 125mS or to shorten it when it is less than that. Adjust VR12 again so that T becomes 4 ± 0.1mS when TP5 is +8 ± 0.1V. Repeat this adjustment until T becomes 125 ± 5mS when TP5 is +3 ± 0.1V.

c. Make sure that T is multiplied by 3.3 to 6.1 when NORMAL/TIME x 5 switch (PSW9) is at TIME x 5 position and that LED indicator (LE11) glows when the key is ON.

LFO Circuit Board

1. LFO Oscillation Circuit

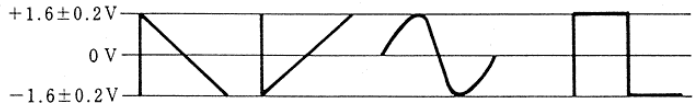
Turn EG–DEPTH volume (PV1) to 0 and SPEED control (PVR2) to S positions and adjust [VR 2] to provide terminal ◺ (③–8) with 0.1 ± 0.02Hz.

Then, adjust [VR 1] to obtain 100 ± 2Hz when SPEED control (PVR2) is turned to F position.

LED indicator will glow according to the number of frequencies.

2. Waveform Conversion Circuit

a. The waveforms shown in Fig. 1, Fig. 2, Fig. 3 and Fig. 4 should be obtained at terminals ◺ (③–8), ◸ (③–7), ∿ (③–9) and ⊓ (④–1) respectively.



b. When LFO/NORMAL switch on TRIGGER is turned to LFO (0V at terminal N (④–2) and the key is turned ON (–7V is applied to terminal KTR (④–3)), the waveform shown in Fig. 5 should be obtained at terminal O ⊓ (③–10) and its frequency should be one half (cycle time is two times that of LFO oscillator.)

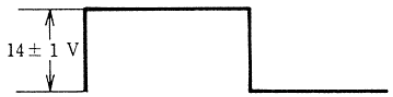
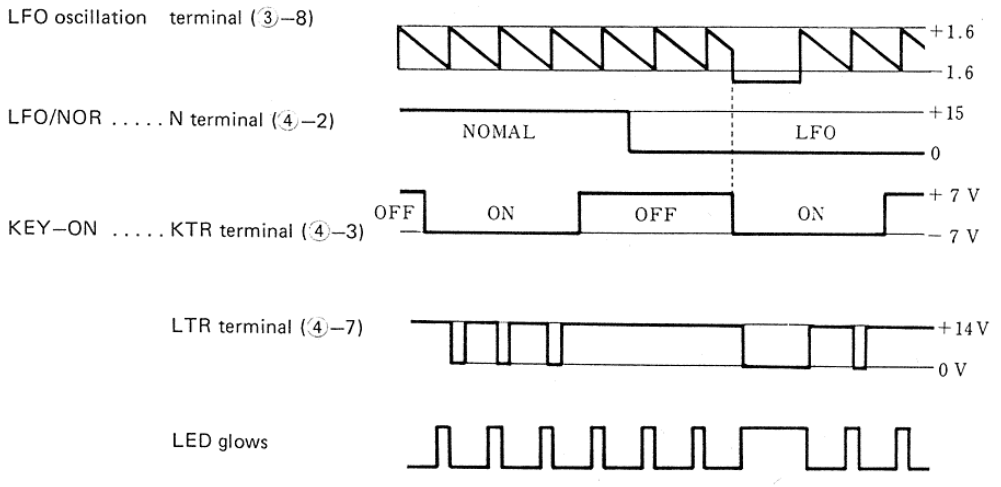


Fig. 5

3. Trigger Circuit

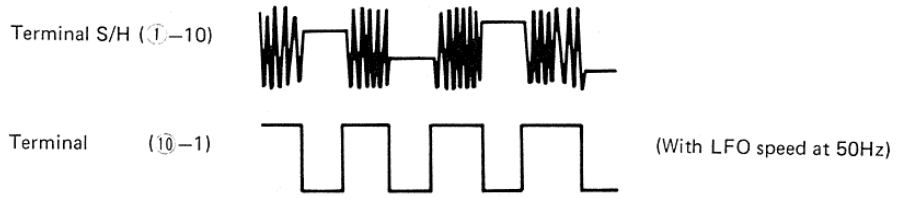
Terminal LTR (④–7) should operate as shown in Fig. 4 under the following conditions:



4. Noise Generator Circuit

a. Adjust [VR 3] to obtain 5 ± 1 Vp-p (2 dBm) output at terminal NI (2 –1).

b. Adjust [VR 4] so that voltage fluctuates at terminal S/H (①–10) to an equal degree above and below 0V as the center, as illustrated below:



5. EXT Pre-amplifier Circuit

a. Set FEET on VCO1 to 8', ⌒ VCO1 on VCA1 to 10, and all others to 0, and turn EG/HOLD selector switch to HOLD.
Then, set BALANCE on PN3 to 1 and adjust VOLUME to provide OUTPUT 1 with a 20mV (–40 dBm) output level when key C_4 is turned ON (1053Hz output).
Now, connect OUTPUT 1 to EXTERNAL–IN by using a guitar lead (20mV, 1053Hz is applied to terminal ESI (②–7).

b. After the completion of the setting mentioned in paragraph 5–a, 120mV output should be obtained at terminal 0(②–5) when SIGNAL LEVEL (PVR4) is turned to 10. Also, 1.25V output should be presented at terminal –20 (②–3).

6. EXT Trigger Circuit

In addition to the same setting as mentioned in paragraph 5–(a), set TRIGGER LEVEL (PVR3) to 10 and –20/0 selector switch on the rear panel to the 0 position. When SIGNAL LEVEL is set so that a voltage of +60 ± 5mV is applied at terminal ETI (④–6), 0 ± 0.2V output should appear at terminal ETO (④–5).

In addition, when SIGNAL LEVEL is set to 0, +15V output should be obtained at terminal ETO.

PRA Circuit Board

1. **Amplifier Circuit**

   Set the PN3 VOLUME to MAX and make sure that an input signal of about 0.3V is applied to terminals 1I (①–7) and 2I (①–9) respectively when the key is turned ON. Then, adjust [VR1] and [VR2] so that 0.6V signal appears at terminals 1H (①–5) and 2H (①–13) respectively.

   At this stage, 100mV output must be obtained from terminals 1L (①–2) and 2L (①–11) respectively, and also 0.6V output from 1 + 2H (②–2) and 50mV output from 1 + 2L (①–15) terminals.

2. **Headphone Amplifier Circuit**

   When a set of headphones (8 ohm) is connected to the PHONES jack on PN3, 250mV output should be obtained from terminals HR (②–13) and HL (②–12).

3. **Initial Clear Circuit**

   Connect either a set of headpnones or a guitar amplifier, turn the key ON and make sure that a sound is produced. Turn the main switch OFF and then turn it ON after 10 seconds. A sound should be heard about 8 seconds after the main switch has been turned ON.

4. **Foot Controller Current Regulation Circuit**

   A +14 ± 1V and −14 ± 1V should be obtained from terminals +X (②–15) and −X (②–14) respectively.

INDEX (目　次)

VCO Circuit Board

1. **Tune Circuit**

   Set the TUNE knob to fully [–] position and [+] position, make sure that +75 ± 5mV and –75 ± 5mV are respectively obtainable at TU (①–1) terminal.

2. **EG Modulator Circuit**

   Set the SEQ/KBD/EXT switch in Envelope Generator 2 to KBD position, AT, DT, RT to S, SL to 10, EG–SELECTOR (PSW1) to C position, EG–DEPTH (PVR3) to 10 and turn a key ON, make sure that 0.8V is obtainable at EG (⑤–13) terminal. (+8V Envelope voltage waveform is fed into C (⑤–78) terminal.)

   Turn the DEPTH (PVR3) knob to the left gradually and make sure the voltage at EG terminal is gradually diminished, resulting in 0 ± 0.1V when the knob is fully turned to 0 position.

3. **DE–TUNE Circuit**

   a. Put the isoration plug into KEYVOLT–IN (J5) on rear panel, connect the KV (④–9, 10) terminal to EK (③–1 ~ 4) terminal with jamper wire and set the MOD VCO2 (PVR4) to 0, then adjust [VR 1] so that 0 ± 50μV or less is obtained at CP1.

   b. Under the condition of item 3–(a), adjust [VR 2] so that 0 ± 50μV or less is obtainable at CP2.

   c. Remove jamper wire and isoration plug next. Let SEQ/KBD switch (PSW4, 5) at KBD, set EG–DEPTH (PVR3) to 0 and turn C_6 key ON after TU (①–1) terminal is set to 0.000V by TURN Volume. (at the time there is 2.000V at KV terminal.)

   When CP2 is set at 2.000V by DE–TUNE volume make sure that there is 2.000V at IC6, 7 second pin and also is 166.8mV at IC6, 7 second pin when F_2 key is ON.

4. **Voltage Control Oscillator Circuit 1 (VCO1) & Wave Shape Convertor Circuit 1 (WSC1)**

   a. Set both VCO1 and VCO2 SEQ/KBD switches to KBD side, MOD DEPTH (PVR9, 10) are 10, FEET 1 (PSW2) at 2' and turn the TUNE (PVR1) volume untill 0.000V is present at TU (①–1) terminal. Then adjust DE–TUNE (PVR2), when F_2 key is pressed, so that the voltage at CP3 is same as that of CP4 (166.8mV). Next, make sure that voltage of 2.000 ± 0.001V is present at CP3 during C_6 key is ON.

   b. After the above setting is completed, adjust [VR 4] to achieve ◺ 1 (④–6) terminal output frequency of 8429Hz when the C_6 key is ON (KV terminal is 2 ± 0.001V).

   c. Adjust [VR 3] to achieve 1053.6Hz when the C_3 key is ON (KV terminal is 250 ± 0.1mV).

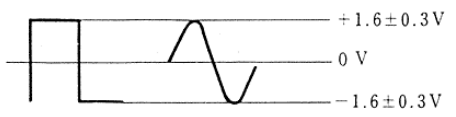
   Note: Repeat (b) and (c) above so that each frequency variation is within 0.1% even when switching.

   d. Check that the frequency is in accordance with the chart below when FEET 1 (PSW2) is switched, as in 4–(b) (i.e., MOD–DEPTH, PWM1, PW1 are 0 and 50%).

FEET	Frequency (Hz)
2'	8429
4'	4215
8'	2107
16'	1053.6
32'	526.8
64'	263.4

within ±0.1%

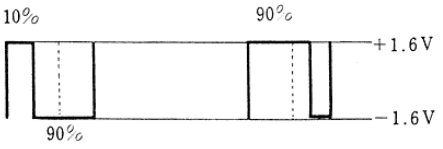
Note: The output indicated below should be present at the ⊓ 1 (④–7) and ∿ 1 (④–5) terminals when the frequency is the same as the ◺ 1 terminal.



5. PW, PWM Circuit

a. Switch the C_6 key ON with FEET 1 (PSW2) at 16', MOD FUNCTION (PSW6) at ∿ and MOD–DEPTH (PVR9) at 10; the frequency should change between 965 and 1150Hz when 3.2Vp-p ∿ wave is added to the ∿ (⑥–1.2) terminal (when the voltage at the ∿ terminal is shifted between +1.6V and –1.6V, the frequency will vary between 965 and 1150Hz). At this time, if the MOD –DEPTH (PVR9) is turned to the left little by little, the frequency variations become less and less; if it is turned all the way to the left, the original frequency (1053.6 ± 1Hz) should appear.

b. Be sure the 3.2Vp-p ∿ wave is added to the ∿ (⑥–1.2) terminal. When PWM1 (PVR7) is at 10, the ⊓ 1 (④–7) terminal receives 90 ~ 10 ± 9% duty voltage. Then, when PWM1 (PVR7) is returned to 0, then when PW1 (PVR5) is 90% the ⊓ 1 waveform duty voltage is 90 ± 9%.



When +1.6V input
When PW1 is 90%

When –1.6V input

Note: Inverted wave is fed out from the rear panel OUTPUT.

6. Voltage Control Oscillator Circuit 2 (VCO2) & Wave Convertor Circuit 2 (WSC2)

a. As in 4–(a), set FEET 2 (PSW3) to 4'. With the C_6 key ON (KV terminal; 2.000V) adjust [VR 8] for 4215Hz at ⟍ 2 (④–3) terminal.

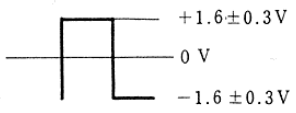
b. Then, with the C_2 key ON (KV terminal; 250.0mV) adjust [VR 7] for 526.8Hz.
Note: Repeat (a) and (b) above so that each frequency variation is within 0.1% even when switching.

c. As in 6–(a), check that the frequency is as indicated in the chart below when FEET 2 (PSW3) is switched.

FEET	Frequency (Hz)
4'	4215
8'	2107
16'	1053.6
32'	526.8
64'	263.4
128'	131.7

within ±0.1%

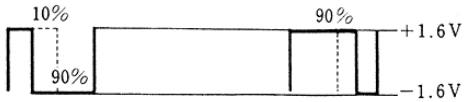
Note: The waveform shown below should be obtained at the ⊓ 2 (④–4) terminal at the same frequencies as ⟍ 2 terminal.



7. PW, PWM Circuit

a. Switch the C_6 key ON, the FEET 2 (PSW3) to 16', MOD FUNCTION (PSW7) to ⋀⋁ and MOD–DEPTH (PVR10) to 10. When a 3.2Vp-p ⋀⋁ wave is fed to the ⋀⋁ (⑥–1.2) terminal the frequency should shift more than 970 ~ 1160Hz (when the voltage at the ⋀⋁ terminal is shifted between +1.6V and –1.6V the frequency will vary between 970 and 1160Hz). At this time, if the MOD–DEPTH (PVR10) is turned to the left little by little, the frequency variations become less and less; if it is turned all the way to the left, the original frequency (1053.6Hz) should appear.

b. Check that a 3.2Vp-p ⋀⋁ wave is added to the ⋀⋁ (⑥–1.2) terminal. When PWM2 (PVR8) is at 10, the ⊓⊔ 2 terminal (④–4) receives 90 ~ 10 ± 9% duty voltage. Then, when PWM2 is returned to 0 and PW2 (PVR6) is at 90%, the ⊓⊔ 2 waveform duty voltage is 90 ± 9%.



When +1.5V input
When PW2 is 90%

When –1.6V input

Note: Inverted wave is fed out from the rear panel OUTPUT.

8. FM Modulation Circuit

a. Set the MOD–VCO2 (PVR4) to 10. Then, when the C_6 key is switched ON (KV terminal; 2 ± 0.001 V) adjust [VR 6] at TP1 for a value according to Fig. 1.
Now, when the C_3 key is switched ON (KV terminal; +250 ± 0.1mV), adjust [VR 5] according to Fig. 2.
Repeat these adjustments, making sure there is no deviation in the adjusted value, even during switching.

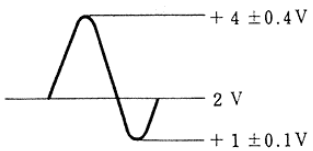


Fig. 1

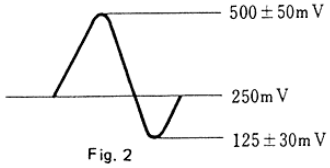


Fig. 2

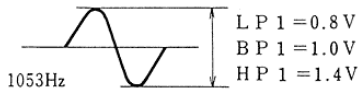
b. Switch the C_6 key ON (KV terminal, +2 ± 0.001V). When MOD–VCO2 (PVR4) is set to 0, +2 ± 0.002V should appear at TP1. In this condition, when DE–TUNE (PVR2) is at the [+] side, +3 ± 0.1V should appear at TP2; when it is at the [–] side, +1.5 ± 0.1V should appear.

VCF Circuit Board

1. Voltage Control Filter Circuit (VCF1)

a. Set INPUT (PSW1) to ⌐ 1 and LEVEL 1 (PVR1) to 10, LEVEL 2 (PVR2), MOD DEPTH (PVR9) and EG–DEPTH (PVR11) to 0 respectively. Then set the VCO1 FEET to 4' and turn the C_4 key ON. Add a 3.2Vp-p ⌐ wave to the ⌐ 1 (①–1) terminal and then adjust CUT OFF FREQ (PVR7) and RESONANCE (PVR5) for +5V at TP2 and TP4.

b. Under the same conditions as in 1–(a), adjust [VR 1] for peak level and [VR 2] for peak point so that an 0.8Vp-p waveform is present at the LP1 (④–7) terminal.
Next, the BP1 (④–6) terminal should have a 1.0V output waveform, and HP1 (④–5) terminal should have 1.4V (check that the KV voltage (+500 ± 5mV) is added to the second pin of IC_2).



c. Leave adjustments as in 1–(b) and use the CUT OFF FREQ (PVR7) to adjust for a TP2 voltage of +7 ± 0.1V. Then turn the B_5 key ON; when the KBD FOLLOW (PVR3) is set for 500mV at the second pin of IC_1 the LP1 level should just peak.
Next, when TP2 voltage is +3 ± 0.1V turn the B_2 key ON. When the KBD FOLLOW (PVR3) is used to set for 500mV at the second pin of IC_1 the LP1 level should peak.

d. Return the settings to the 2–(a, b) condition. When the MOD FUNCTION (PSW4) is set to ∧∨ and MOD DEPTH (PVR9) to 10 check the cutoff frequency by listening to the sound according to the input ∧∨ wave.

e. Set EG1 ~ 3 to any position and EG DEPTH (PVR11) to approximately center position. Peak frequency should vary according to the EG waveform when the EG SELECTOR (PSW6) is switched from A to E.

2. Voltage Control Filter Circuit (VCF2)

a. Set INPUT (PSW3) to ⌐ 2 and both MOD DEPTH (PVR10) and EG DEPTH (PVR12) to 0. Then set the VCO2 FEET to 4' and turn the C_4 key ON. Add a 3.2Vp-p ⌐ wave to the ⌐ 2 (①–2) terminal and then adjust CUT OFF FREQ (PVR8) and RESONANCE (PVR6) for +5V at TP3 and TP5.

b. Under the same conditions as in 2–(a), adjust [VR 3], for peak level and [VR 4] for peak point so that an 0.8Vp-p. Waveform is present at the LP2 (④–3) terminal.
Next, the BP2 (④–2) terminal should have a 1.0V output waveform, and HP2 (④–1) terminal should have 1.4V (check that the KV voltage (+500 ± 5mV) is added to the second pin of IC_2).